FIG. 1

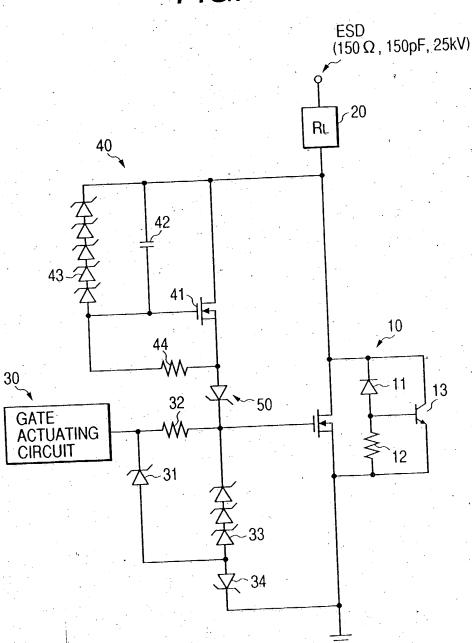


FIG. 2A

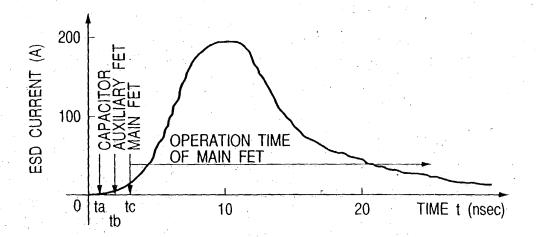


FIG. 2B

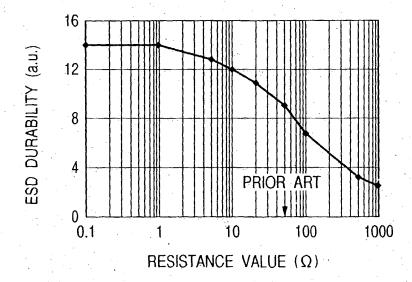
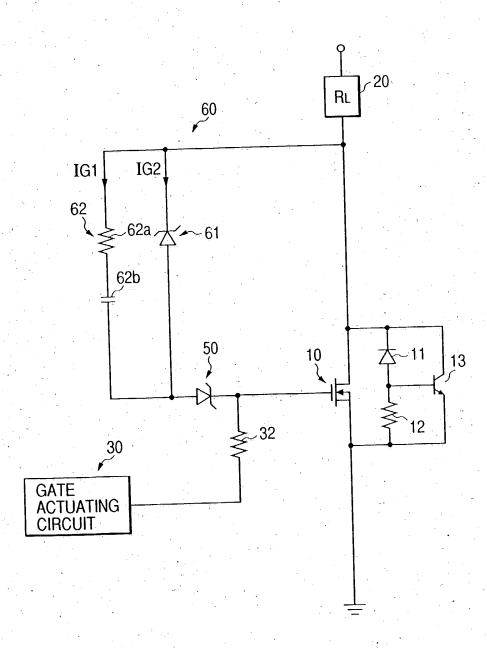


FIG. 3



Title: Semiconductor Device Including A Surge Protecting Circuit

Inventor: Kenji Kohno Atty. Ref. No.: 4041P-000020/DVA

FIG. 4

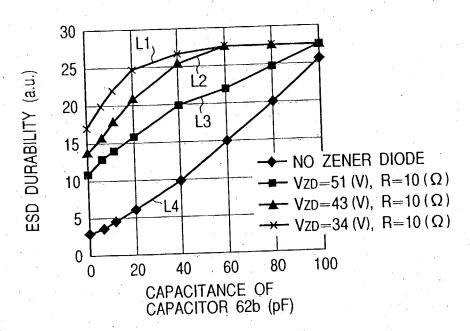


FIG. 5

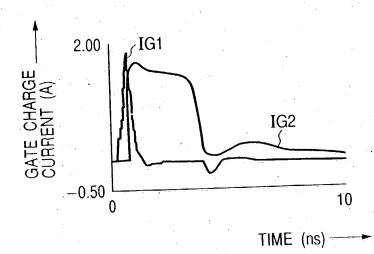
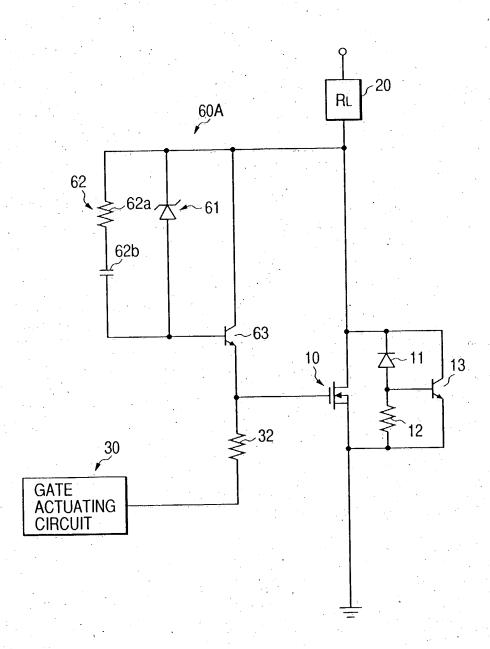
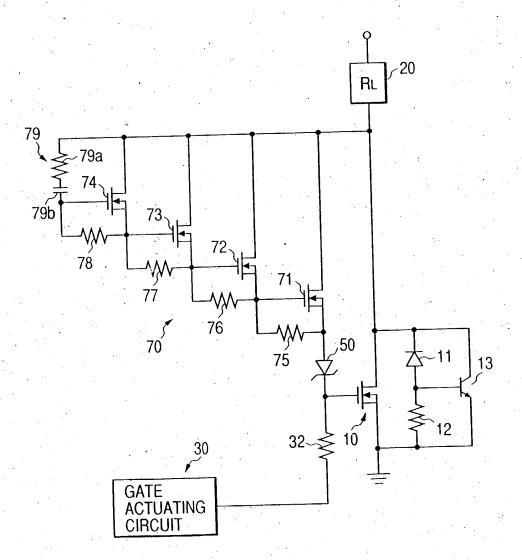


FIG. 6



6/.29

FIG. 7



Title: Semiconductor Device Including A Surge Protecting Circuit Inventor: Kenji Kohno

Inventor: Kenji Kohno Atty. Ref. No.: 4041P-000020/DVA

FIG. 8

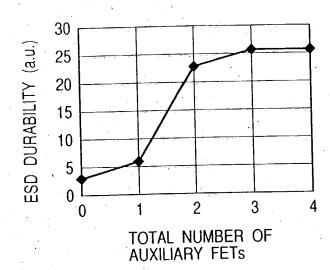


FIG. 10

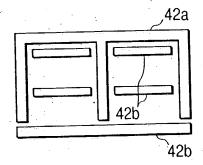


FIG. 11 PRIOR ART

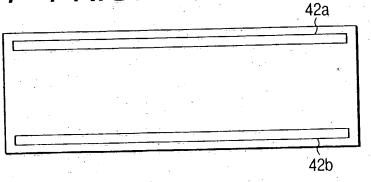


FIG. 9

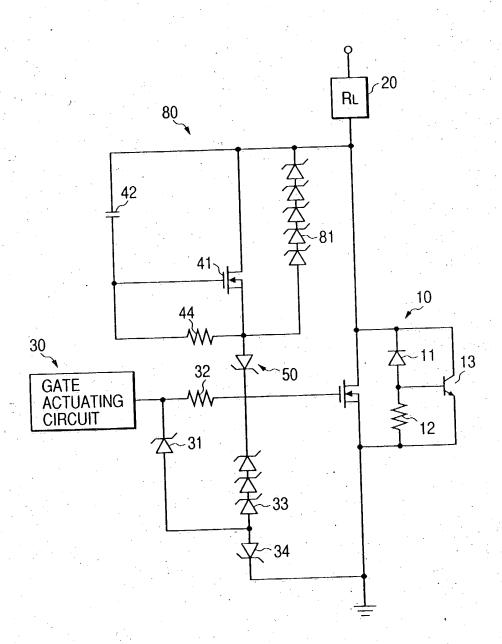


FIG. 12A

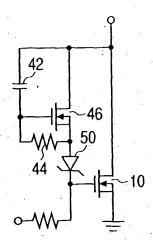


FIG. 12B

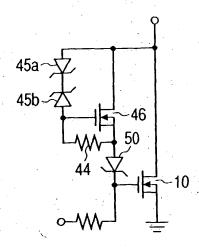
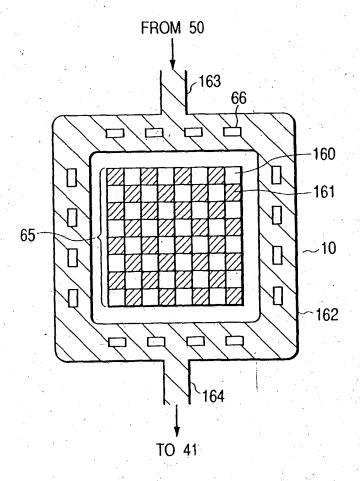


FIG. 14



10 / 29

FIG. 13A

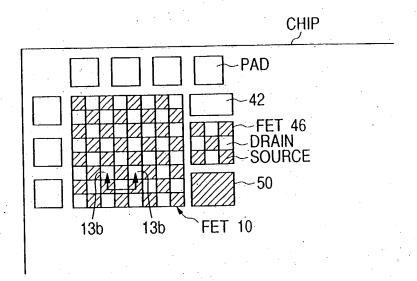
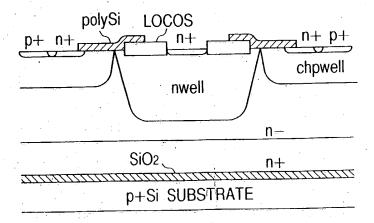


FIG. 13B



Inventor: Kenji Kohno Atty. Ref. No.: 4041P-000020/DVA

FIG. 15A

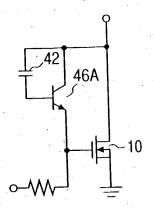


FIG. 15B

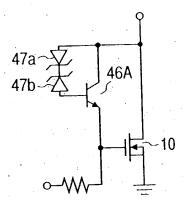


FIG. 16A

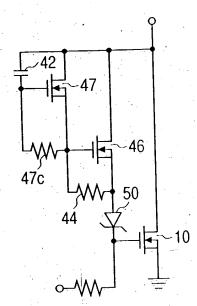
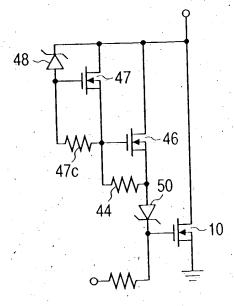


FIG. 16B



Title: Semiconductor Device Including A Surge Protecting Circuit

Inventor: Kenji Kohno Atty. Ref. No.: 4041P-000020/DVA

FIG. 17A

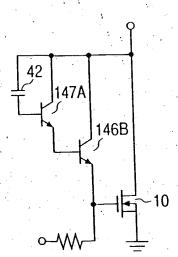


FIG. 17B

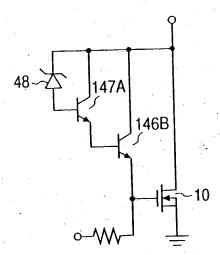


FIG. 18A

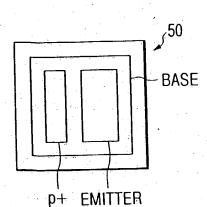
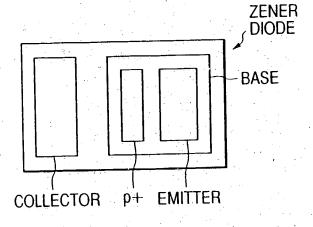
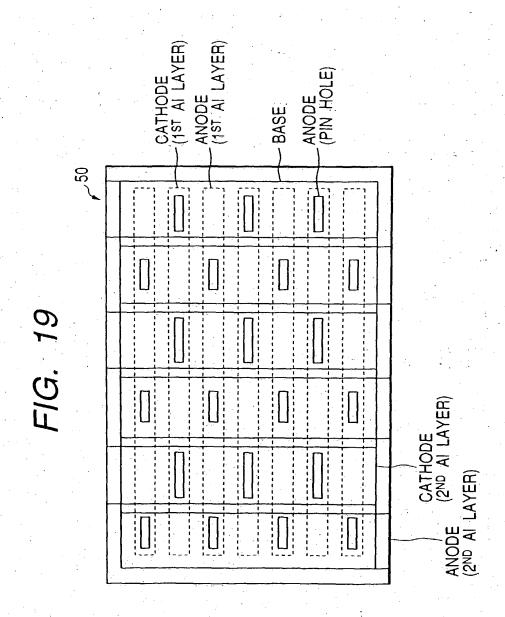


FIG. 18B PRIOR ART





Title: Semiconductor Device Including A Surge Protecting Circuit

Inventor: Kenji Kohno Atty. Ref. No.: 4041P-000020/DVA

FIG. 20A

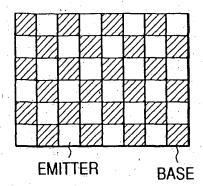


FIG. 20B

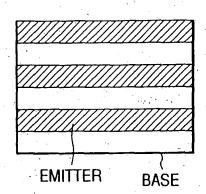


FIG. 21

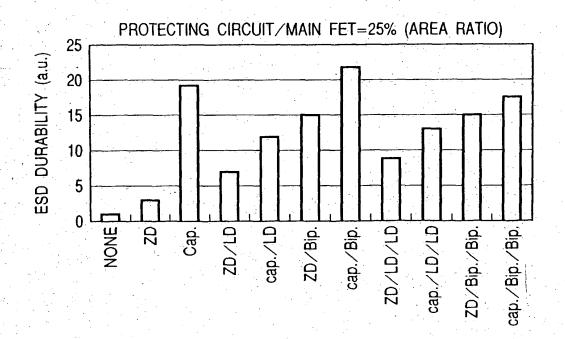
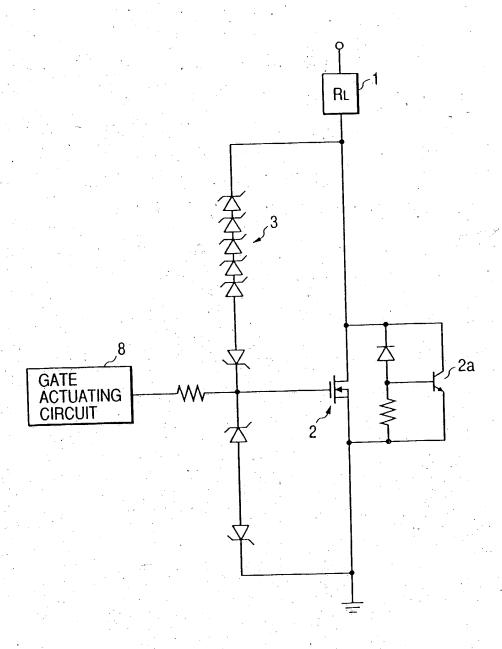
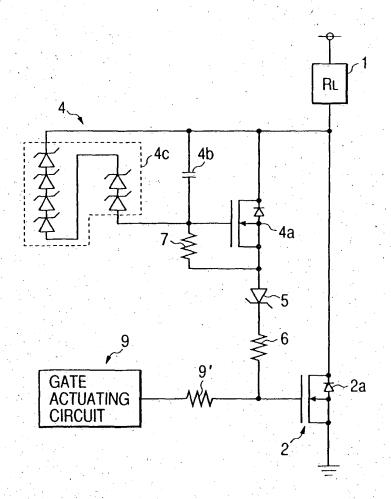


FIG. 22 PRIOR ART



16 / 29

FIG. 23 PRIOR ART



17/29

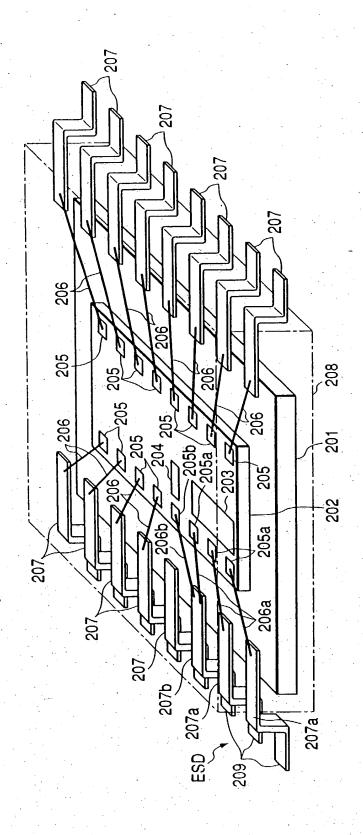


FIG. 25

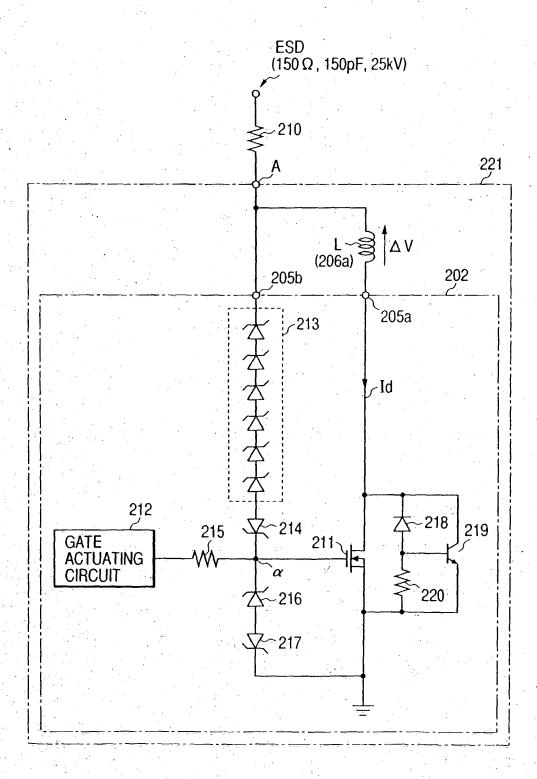


FIG. 26

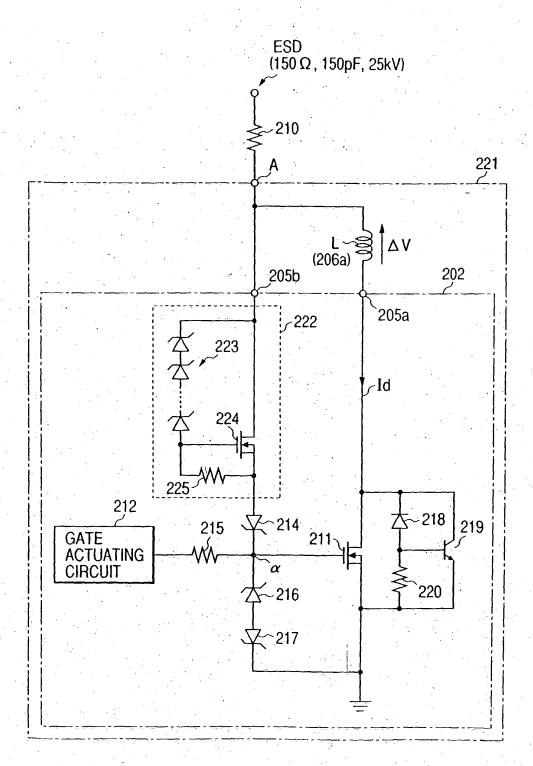


FIG. 27

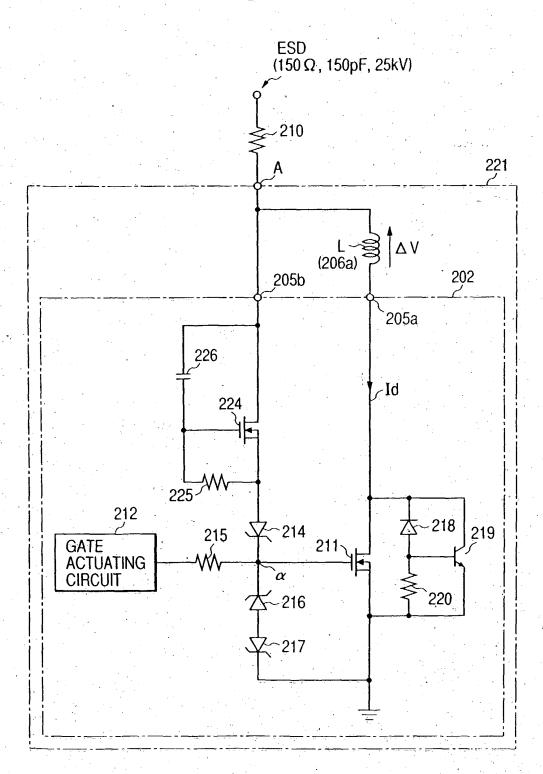
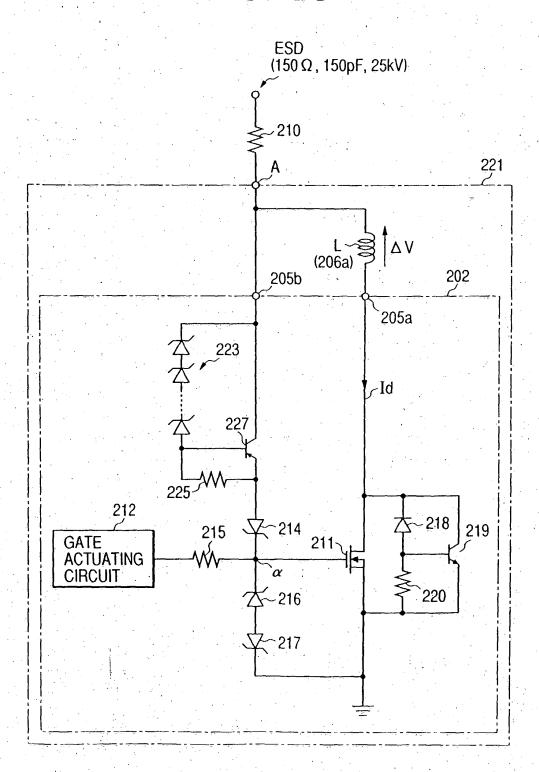


FIG. 28



22,/29

FIG. 29

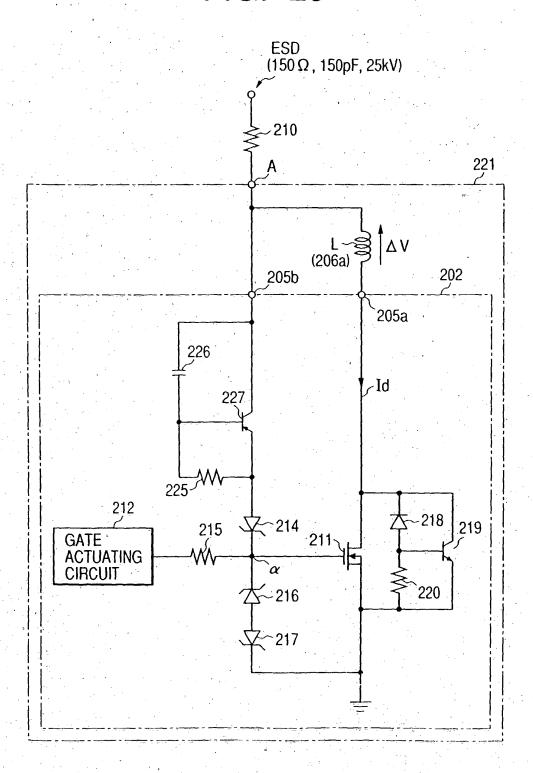
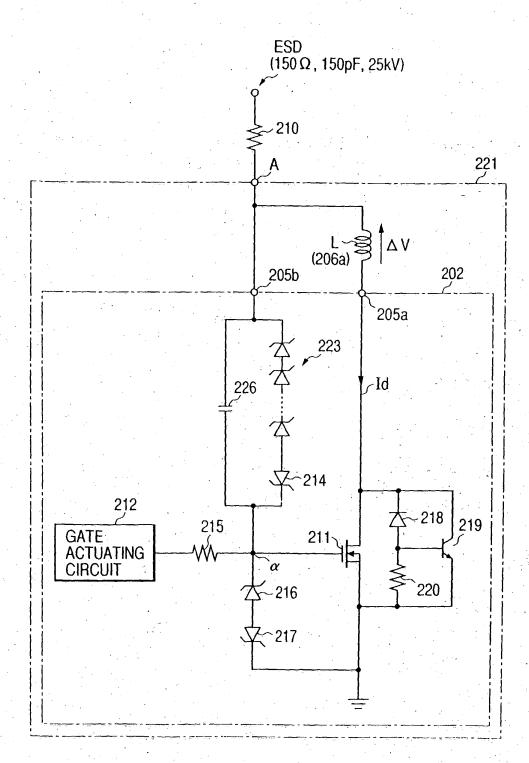
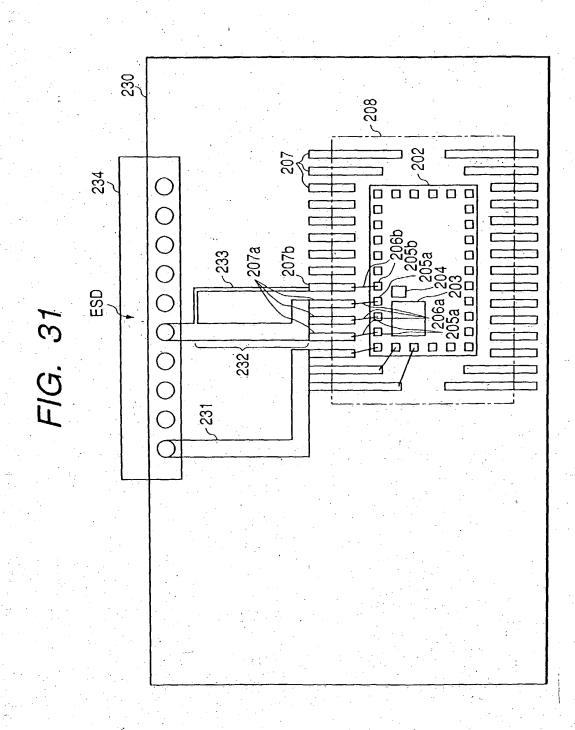
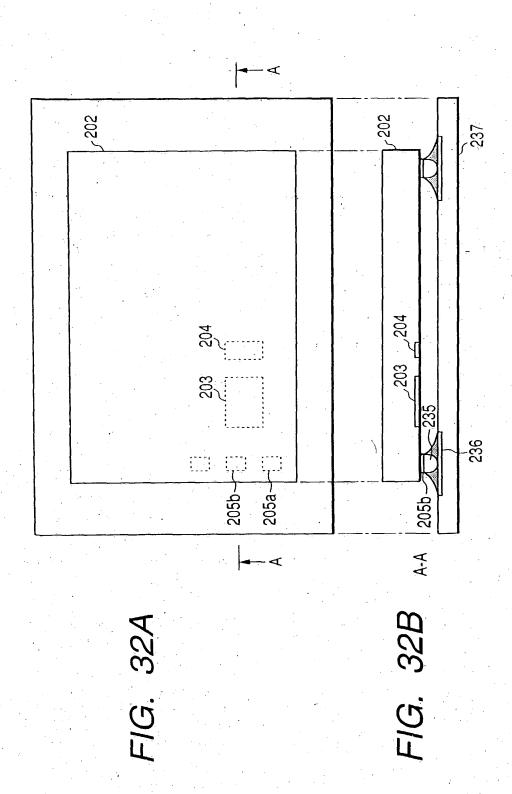
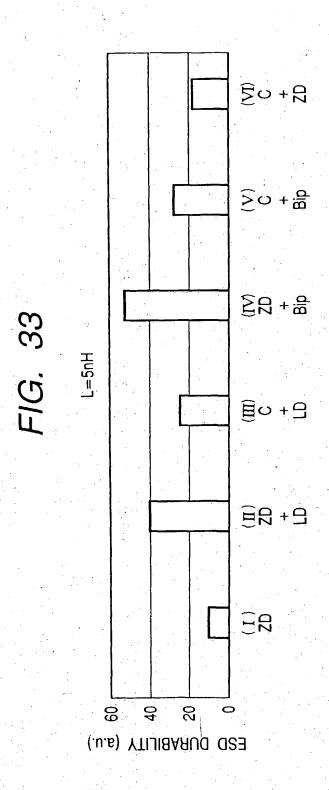


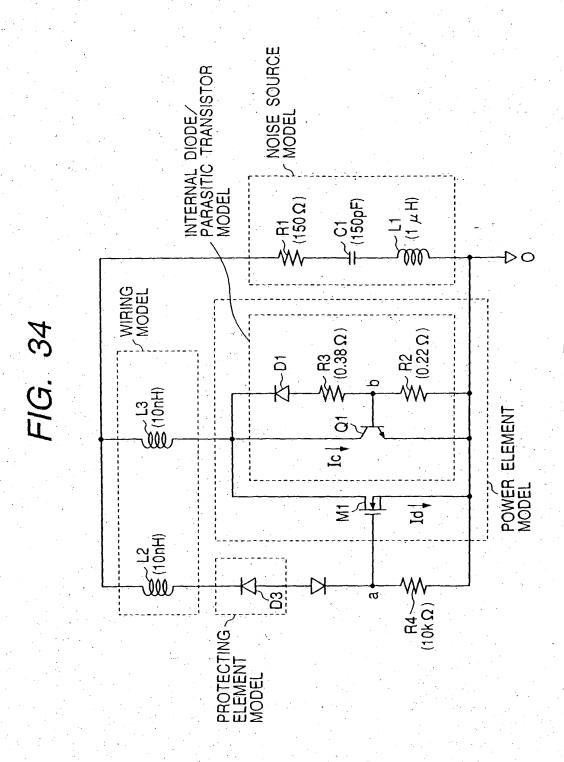
FIG. 30

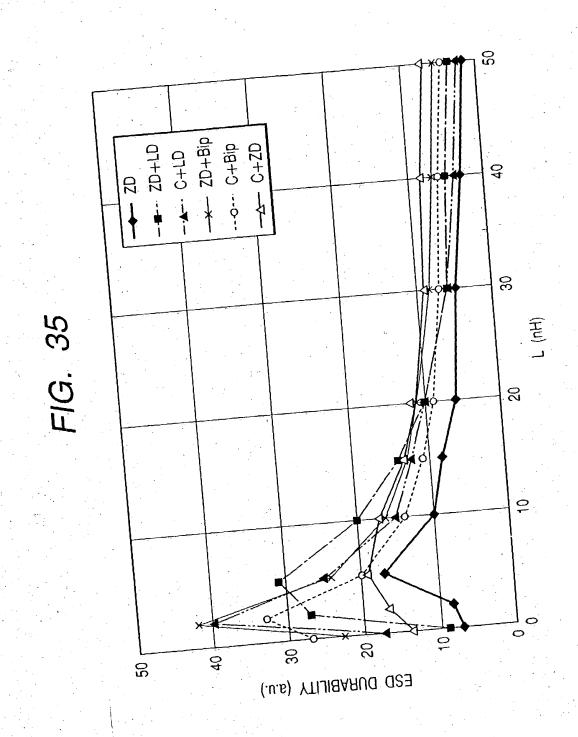












Title: Semiconductor Device Including A Surge Protecting Circuit Inventor: Kenji Kohno

Atty. Ref. No.: 4041P-000020/DVA

FIG. 36A

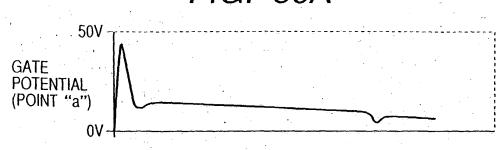


FIG. 36B

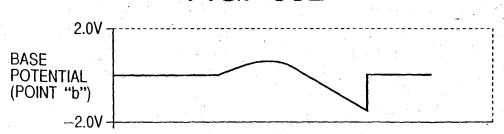


FIG. 36C

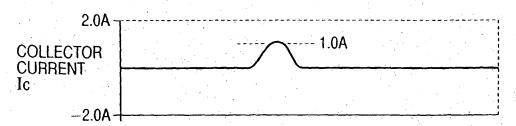


FIG. 36D

